A5

FIG. 8 are denoted by like reference numerals and descriptions thereof are omitted. Only the differences from FIG. 8 will be described below.

IN THE CLAIMS

Please amend Claims 1 and 12 to read as follows:

A6

1. (Amended) A semiconductor device having active regions connected together by interconnect layers comprising:

a semiconductor substrate;

first and second transistors each having a gate electrode and a pair of active regions, the pair of active regions being formed in the semiconductor substrate;

an isolation region formed between the first and second transistors in the semiconductor substrate for isolating the first and second transistors from each other;

at least one slit formed in a top surface region of the isolation region to allow those paired active regions of the first and second transistors which are opposed to each other with the isolation region interposed therebetween to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region, the first, second and third portions being made integral with one another, and the interconnect layer having a top surface which is lower than a top surface of the gate electrode.

A7

12. (Amended) A semiconductor device having active regions connected together by an interconnect layer comprising:

a semiconductor substrate;

first and second MOS transistors each having a gate electrode and a pair of active regions, the pair of active regions being formed in the semiconductor substrate;

an isolation region formed between the first and second MOS transistors in the semiconductor substrate for isolating the first and second MOS transistors from each other;

at least one slit formed in a top surface region of the isolation region to allow paired active regions of the first and second MOS transistors, which are opposed to each other with the isolation region interposed therebetween, to communicate with each other through it, the slit having inner walls and a predetermined width;

a conductive layer formed on the inner walls of the slit;

a gate electrode of another MOS transistor formed above the isolation region; and

an interconnect layer having first and second portions respectively formed on the paired active regions of the first and second MOS transistors so that each of them is electrically connected with a corresponding one of the paired active regions, and a third portion formed along the slit on the isolation region, the first, second and third portions being made integral with one another, and the interconnect layer having a top surface which is lower than a top surface of the gate electrode.

REMARKS

Favorable reconsideration of this application is respectfully requested.

The specification is amended by the present response to correct for minor informalities. The changes made to the specification are deemed to be self-evident from the original disclosure, and thus are not deemed to raise any issues of new matter.